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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,199	09/15/2003	Ting-Shing Wang	11438-US-PA	2198

31561 7590 05/25/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER
VU, DAVID

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,199	WANG, TING-SHING	
	Examiner	Art Unit	
	DAVID VU	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *1-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-26 and 35-38* is/are rejected.

7)☒ Claim(s) *27-34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/15/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/ Restriction

1. Applicant's election without traverse of Group II (Claims 23-38) on 03/31/2005 is acknowledged.

Since Applicant cancelled all of the claims to the non-elected invention, the restriction requirement is deemed moot.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 23-26 and 35-38 are rejected under 35 U. S. C. 102(e) as being anticipated by Mandelman et al. (US 6,777,737, herein after Mandelman).

Regarding claims 23 and 35, Mandelman discloses a method for fabricating a DRAM array, comprising: patterning a semiconductor substrate to form rows and columns of pillars thereon (fig. 7A); forming a capacitor on a lower portion of a sidewall of each pillar (col. 4, lines

49-65); partially filling spaces between the pillars with a first insulating material 36 to cover the capacitors (col. 5, lines 22-30 and fig. 5); forming a gate structure of a transistor on the sidewall of each pillar above the first insulating layer 36, the gate structure comprising a gate electrode 40 and a gate insulating layer 38 between the pillar and the gate electrode 40 (fig. 6); forming a first doped region 48 of a transistor in the sidewall of each pillar coupling with the capacitor on the sidewall of the same pillar; forming a second doped region 48 of a transistor in a top portion of each pillar (fig. 11); filling the spaces between the pillars with a second insulating material 56/64/62 to cover the transistors; forming a plurality of bit lines over the substrate, wherein each bit line is electrically connected to the second doped regions 48 of the transistors in one row (col. 7, lines 43-53 and fig. 14); and forming a plurality of word lines 60 over the substrate, wherein each word line 60 is coupled with the gates 40 of the transistors in one column (col. 7, lines 35-42 and fig. 14).

Regarding claim 24, Mandelman discloses forming the capacitor on the lower portion of the sidewall of each pillar comprises: doping a surface layer of the substrate and the lower portions of the sidewalls of the pillars to form a common electrode 26; forming a dielectric layer 28 surrounding the lower portion of the sidewall of each pillar; and forming an upper electrode 32 covering the dielectric layer 28 for coupling with a corresponding first doped region (col. 4, lines 49-65 and fig. 4).

Regarding claim 25, Mandelman discloses a top of the upper electrode is higher than a top of the dielectric layer, and forming the capacitor on the lower portion of the sidewall of each pillar further comprises: forming a collar insulating layer 30 on the sidewall of the pillar above the dielectric layer 28 before the upper electrode is formed, so that the collar insulating layer

surrounds the pillar and is covered by an upper portion of the upper electrode 32 (col. 4, lines 49-65 and fig. 4).

Regarding claim 26, Mandelman discloses the upper electrode 32 comprises a doped semiconductor material, and a top portion of the upper electrode above the collar insulating layer directly contacts with the pillar (fig. 6), so that the first doped region is formed via dopant diffusion from the top portion of the upper electrode to the sidewall of the pillar during thermal processes after the upper electrode is formed.

Regarding claim 36, Mandelman discloses wherein the gate electrodes on the pillars of one column are connected via the conductive layer between the pillars of the same column to form the gate line (figs. 10-11), and the step of forming the word lines comprises: forming a dielectric layer over the substrate covering the bit lines; and forming at least one contact through the dielectric layer and a word line on the dielectric layer to electrically connect with the gate line, wherein the contact directly contacts the conductive layer between two pillars of the same column (figs. 12-14 and col. 7, lines 19-42).

Regarding claim 37, Mandelman discloses each bit line is formed with a cap layer thereon; and the method further comprises: forming a protective spacer on sidewalls of each pair of bit line and cap layer before the dielectric layer is formed (figs. 12-14 and col. 7, lines 43-53).

Regarding claim 38, Mandelman discloses the contact and the word line are formed with a damascene process (figs. 12-14 and col. 7, lines 19-42).

Allowable Subject Matter

3. Claims 27-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Vu

May 21, 2005.